Short Papers

Millimeter-Wave Monolithic Power Amplifier for Mobile Broad-Band Systems

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***Abstract*—For personal communication systems, the highest possible integration into monolithic technology of all RF functions are desirable. A frequency band around 60 GHz is assigned for future mobile communication fourth-generation systems (i.e., mobile broad-band systems concept). In this paper, the design and test of two monolithic class-A power amplifiers with 0.15-μm pseudomorphic heterojunction FET (PMHFET) technology is presented. One of the amplifiers is a three-stage cascade 50-Ω amplifier and the second is a balanced amplifier based on the previous one, but matched for integration on a waveguide carrier. A study on the accuracy of the passive elements and discontinuities models at 60 GHz was performed. Models for the microstrip discontinuities were obtained from electromagnetic simulation. In order to choose the best FET bias, a nonlinear model for the PMHFETs devices, based on continuos dc and ac measurements, were derived. For comparison purposes, the FET simulation results with a nonlinear model based on pulsed measurements are also presented. To avoid stability problems, at the device level an *RC* feedback network was introduced. A 1-dB compression point of 18 dBm was measured on-wafer for both amplifiers at 62 GHz with $V_{\mathrm{DSbias}} = 3.5$ V. The three-stage and balanced amplifiers chip sizes are 3 mm $\times$ 1.5 mm and 3 mm $\times$ 4 mm, respectively.**

***Index Terms*—Feedback, large-signal model, MMWIC, PMHFET, power amplifier, V-band.**

I. Introduction

One of the assigned frequency bands for future mobile broad-band systems (MBSs) in Europe is in the 60-GHz range [1] because it is a good choice for microcells due to oxygen absorption.

In this paper, the design and test of 60-GHz monolithic class-A power amplifiers is presented. Two prototypes were fabricated: a three-stage cascaded amplifier and six-transistor balanced amplifier. The balanced amplifier design takes into account the wire bonding since it will be integrated on an MBS system demonstrator. They use pseudomorphic high field-effect transistor (PMHFET) monolithic technology with 0.15-μm mushroom gate length [2] and microstrip structures. In order to stabilize the PMHFETs at lower frequencies, an *RC* feedback network was introduced in parallel with each active device.

Initially, the only available PMHFET model was based on pulsed dc and ac measurements up to 20 GHz and extrapolated to millimeter waves (P-model). However, it was not sufficiently accurate at the device level and it was only reasonably accurate close to the dc-bias point used in pulsed measurements.

Accordingly, to simulate the power amplifier an accurate model for the PMHFET was developed (C-model). The model is based on steady state dc and S-parameters measurements up to V-band. The model takes into account the ac dispersion of the transconductance and output conductance.

Some of the passive element models available at commercially microwave computer-aided design (CAD) simulators [3] are not accurate enough for millimeter-wave circuits design. Accordingly, models for the microstrip discontinuities were obtained from electromagnetic (EM) simulation [4]. The measured values for input and output return loss, output power, and gain are in agreement with the simulations when the C-model for the PMHFETs together with the EM models for the main microstrip discontinuities are used.

For the three-stage cascaded amplifier, an output power greater than 21 dBm at 62 GHz with more than 10-dB gain was achieved with $V_{\mathrm{DS}} = 3.5$ V. The chip size is 3 mm $\times$ 1.5 mm. The balanced amplifier prototype experiments show an output power of 20 dBm at 62 GHz, for an input power of 10.7 dBm. A 1-dB compression point of 18 dBm was measured. The chip size is 3 mm$\times$ 4 mm.

II. Active Device Modeling

In order to perform power simulations, an accurate nonlinear model for the 0.15-μm PMHFET transistor is needed. An available model, obtained from pulsed measurements up to 20 GHz and extrapolated to millimeter waves (P-model), is not sufficiently accurate [5]. Accordingly, a new model was developed (C-model). The model parameters were extracted from classic continuous on-wafer measurements: dc and cold/hot S-parameters.

Device model extrinsic elements were evaluated from S-parameters measurements at zero voltage drain–source bias (cold measurements). Parasitic resistances and inductances were obtained from measurements performed under high gate current conditions, according to Dambrine *et al.* [6], and parasitic capacitances were calculated with the FET biased below pinchoff condition, as proposed by White and Healy [7]. The values of the intrinsic elements were obtained from S-parameters measurements at multibias points at the saturation region, according to Berroth and Bosch [8]. Consequently, this large-signal model is valid over the entire saturation region. This makes it useful for nonlinear simulation of class-A amplifiers. The model topology is presented in Fig. 1.

The proposed current source i_{DS} equation is as follows:

$$i_{\mathrm{DS}}(v_{\mathrm{GS}}, v_{\mathrm{DS}}) = id_1 \cdot id_2 \cdot id_3 \cdot id_4 \tag{1a}$$

$$id_1 = \beta \cdot (v_{\mathrm{GS}} - V_{\mathrm{T}})^Q \tag{1b}$$

$$id_2 = \frac{mn + (mx - mn)}{2}\left[1 - \tanh\left(Sp \cdot (v_{\mathrm{GS}} - V_{\mathrm{GSO}})\right)\right] \tag{1c}$$

$$id_3 = 1 + a_1 \cdot v_{\mathrm{DS}} + a_4 \cdot v_{\mathrm{DS}}^4 \tag{1d}$$

$$id_4 = \tanh\left[\alpha_0 - \alpha_1 \cdot (v_{\mathrm{GS}} - V_{\mathrm{T}})\right] \tag{1e}$$

$$V_{\mathrm{T}} = V_{\mathrm{TO}} - \lambda \cdot v_{\mathrm{DS}}. \tag{1f}$$

Equation (1) parameters were obtained by fitting to dc $I_{\mathrm{DS}}(V_{\mathrm{DS}}, V_{\mathrm{GS}})$ measured characteristics. Function id_1 models the saturated region for v_{GS} values below V_{GS0} (v_{GS} value for maximum transconductance). The typical variation of high electron-mobility transistor (HEMT) transconductance with V_{GS} is modeled appropriately by these sets of equations through id_2. Function id_3 models drain–current increase for large v_{DS} values and id_4

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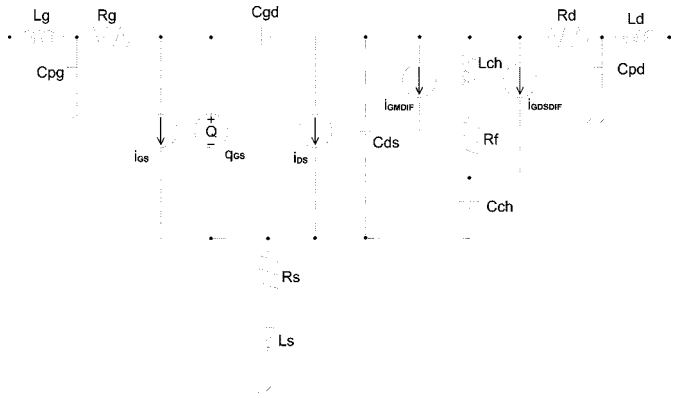

Fig. 1. Lumped-element nonlinear model (C-model) for the 0.15-μm PMHFET.

models the triode region. Since the above $i_{\rm DS}$ equation has continuous derivatives, it is suitable for intermodulation and prediction of higher order harmonic distortion [9].

The derivatives of $i_{\rm DS}$ current source lead to the dc transconductance $(g_{\rm mDC})$ and output resistance $(r_{\rm dsDC})$. The ac transconductance $g_{\rm mAC}$ and output resistance $g_{\rm dsAC}$ were obtained from multibias S-parameters measurements. To take into account frequency dispersion [10], two extra current sources $i_{\rm gmdif}$ and $i_{\rm gdsdif}$ were introduced in parallel with $i_{\rm DS}$ current source [11]. The corresponding equations are

$$i_{\rm gmdif}(v_{\rm GS}) = {\rm Gmdif}_1 \cdot v_{\rm GS} + \left(\frac{{\rm Gmdif}_2}{2}\right) \cdot v_{\rm GS}^2 \tag{2a}$$

$$i_{\rm gdsdif}(v_{\rm DS}) = {\rm Gdsdif}_1 \cdot v_{\rm DS} + \left(\frac{{\rm Gdsdif}_2}{2}\right) \cdot v_{\rm DS}^2. \tag{2b}$$

Their derivatives are equal to $g_{\rm mAC} - g_{\rm mDC}$ and $g_{\rm dsAC} - g_{\rm dsDC}$, respectively. This dispersion correction must only be effective at ac. Therefore, a large capacitance $C_{\rm ch}$ was included in series with the extra current sources. In order to close a dc loop for $i_{\rm gmdif}$ and $i_{\rm gdsdif}$, a resistor $R_{\rm f}$, in series with a choke inductor $L_{\rm ch}$, was included in the model.

Gate–source junction current $i_{\rm GS}$ is modeled by a classical p-n junction equation

$$i_{\rm GS}(v_{\rm GS}) = I_{\rm S} \exp\left(\frac{v_{\rm GS}}{n \cdot V_{\rm th}}\right) \tag{3}$$

in which parameters are obtained from $i(v)$ dc measurements and $V_{\rm th} = kT/q$. Gate–channel charge storage effect is modeled by a function $Q_{\rm GS}(v_{\rm DS}, v_{\rm GS})$ as follows:

$$Q_{\rm GS}(v_{\rm GS}, v_{\rm DS}) = Qgs_1 \cdot Qgs_2 \tag{4a}$$

$$Qgs_1 = \left[\frac{(\max + \min)}{2}\right] \cdot v_{\rm GS} + \frac{(\max + \min)}{2{\rm S}_1} \cdot {\rm In}\left[\cosh\left(S_1 \cdot (v_{\rm GS} - V_{\rm GSCO})\right)\right] \tag{4b}$$

$$Qgs_2 = 1 + \tanh(S_2 \cdot v_{\rm DS}) \tag{4c}$$

$$V_{\rm GSCO} = a + b \cdot v_{\rm DS}. \tag{4d}$$

$Q_{\rm GS}$ expression is calculated by integration after obtaining the $C_{\rm GS}$ expression [13]. Equation (4) parameters were obtained from mathematical fitting of the $C_{\rm GS}$ expression with multiple-bias-point S-parameters. Due to the charge dependence on $v_{\rm GS}$ and $v_{\rm DS}$ voltages, care should be taken to avoid the transcapacitance effect [12]. In saturation region, capacitance $C_{\rm gd}$ is almost constant [13], thus, a constant value was used for the model parameter.

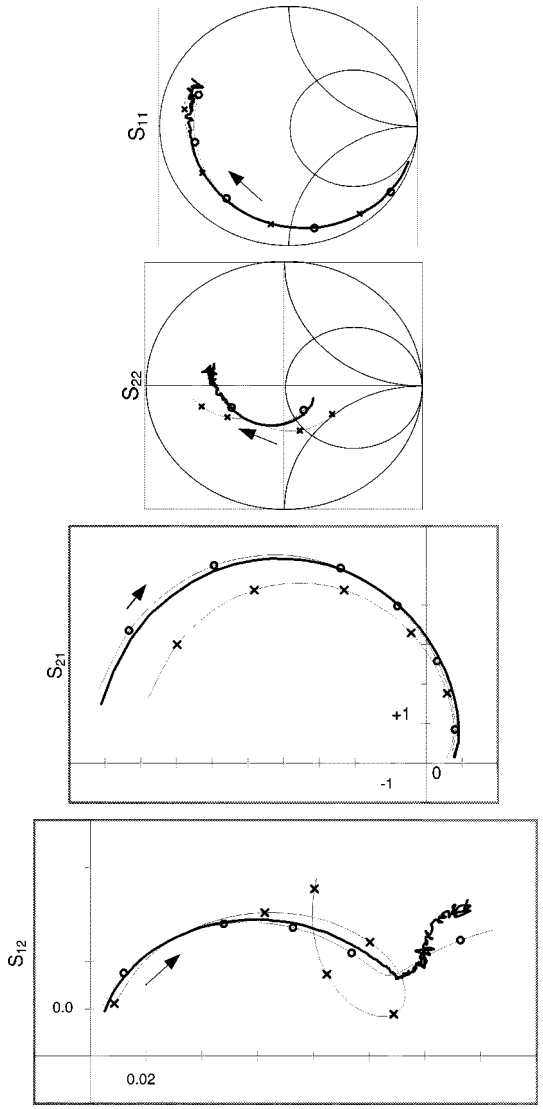

Fig. 2. S-parameters of 6 × 40 μm PMHFET ($I_{\rm D} = 64.8$ mA and $V_{\rm DS} = 3.5$ V) from 1 to 75 GHz (the arrow shows frequency increase): measured (—) and simulated with C-model (–o–) and with P-model (–×–).

For the multibias S-parameters and dc measurements, an automatic bench was implemented. All the test instruments have IEEE 488 bus capability and a desktop computer was used to control the acquisition and processing of the data. Fig. 2 presents the comparison between the S-parameters obtained from the model and measurements for 6 × 40 μm gatewidth PMHFET at a typical power class-A bias point ($I_{\rm D} = 64.8$ mA, $V_{\rm DS} = 3.5$ V).

The reduced accuracy of the P-model at 60 GHz should be associated with the bias conditions, which are not the same as during the extraction of the model parameters and with the maximum frequency of 20 GHz of the available pulsed S-parameters test set. The nonlinear model can be used to extract accurately device S-parameters in the saturation region for any bias point. Thus, this large-signal model is valid over the entire saturation region, being useful for nonlinear simulation of class-A amplifiers.

III. Passive Devices

In this section, a study of the available passive elements models accuracy at millimeter wave (up to 75 GHz) is discussed. When necessary,

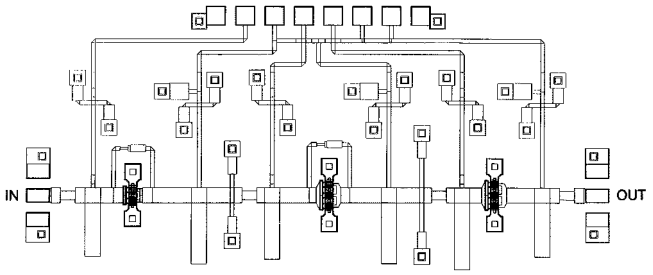

Fig. 3. Three-stage power-amplifier layout.

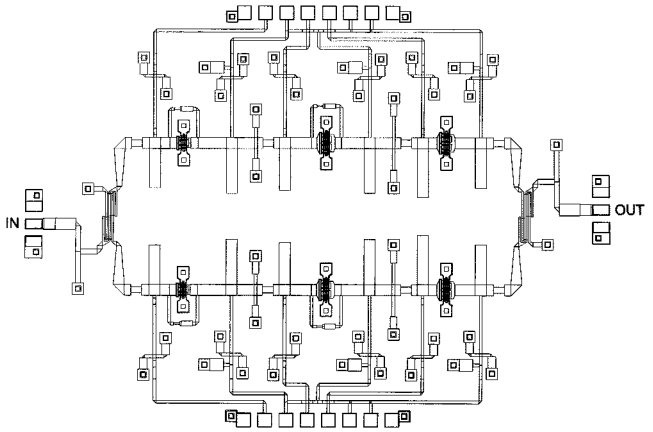

Fig. 4. Balanced amplifier layout.

improved models were developed. The study was based on EM simulation [14] and on wafer measurements with test structures.

The scattering parameters of the metallic resistor, metal–insulator–metal (MIM) capacitor, air bridge, microstrip line, open stub, radial stub, and pads only show a significant difference between the foundry models and the EM simulations on their phase at 75 GHz. At 60 GHz, the difference is always less than 5°, allowing the use of the available models [13].

The ground via also presents significant differences on the phase. A difference of 22° was obtained at 65 GHz, but a slight increase on the via model inductance can be introduced to compensate this inaccuracy. However, it was noticed that when the via is included on a larger circuit, e.g., on a microstrip bias network, the changes on the network input return losses are not significant.

The worst models were those of the microstrip T-junctions and cross junctions. Significant differences were noticed, not only on the phase, but also on the magnitude of the transmission and reflection parameters. One approach to solve the problem is to correct the available models as was proposed by Vaz *et al.* [4]. Another possible solution is to simply characterize those discontinuities by an S-parameters file obtained with an EM simulator [14]. This second approach was used in this paper.

IV. Power-Amplifier Design

A. Three-Stage Amplifier

Usually, millimeter-wave transistors are conditionally stable at lower frequency due to their large gain. In order to stabilize the transistors without the need of complex lossy matching networks, which are bulky and with several discontinuities, simple *RC* series networks in parallel feedback at each transistor were used. With this technique, unconditionally stable cells with a low-gain reduction at millimeter wave

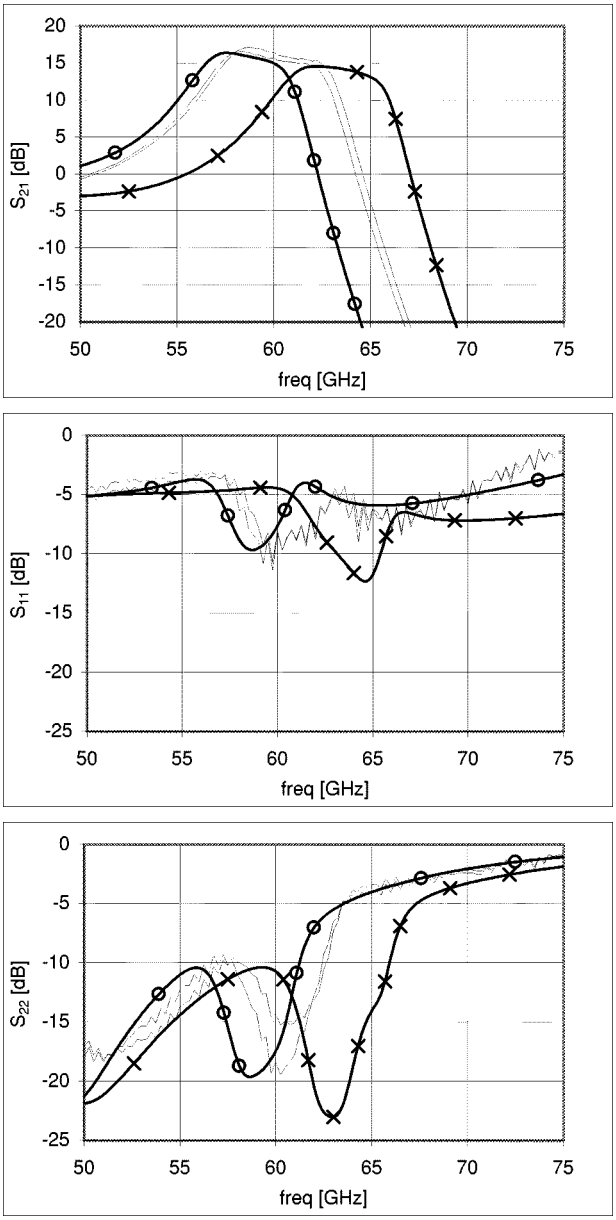

Fig. 5. Small-signal scattering parameters magnitude for the three-stage power amplifier ($I_{\rm D} = 250$ mA and $V_{\rm DD} = 3.5$ V). Experimental results of two chips of the same wafer (—), simulations with EM discontinuities models (–o–), and with MDS discontinuities models (–×–).

(∼1 dB per device) were obtained for maximum gain and for maximum output power. Single-stage amplifiers (with only one transistor) were designed with the elementary cells and input/output 50-Ω microstrip line/stub matching networks. Transistors with 4 × 40 μm and 6 × 40 μm gatewidth were studied.

In order to obtain the required transducer power gain ($G_{\rm T} \geq 10$ dB) from 62 to 63 GHz [1], an amplifier with three cells in cascade was designed and optimized. Fig. 3 presents the 3 mm × 1.5 mm layout of the three-stage power amplifier.

Since the output stage was stable without feedback, the *RC* feedback network was removed from the last transistor to increase the overall gain and output power.

The bias networks use $\lambda/4$ high impedance transmission lines. In order to decouple the circuit from the external bias structure, at the $\lambda/4$ line edge, a good RF short circuit was introduced using two MIM capacitors in parallel. Gate-bias network includes a small resistance

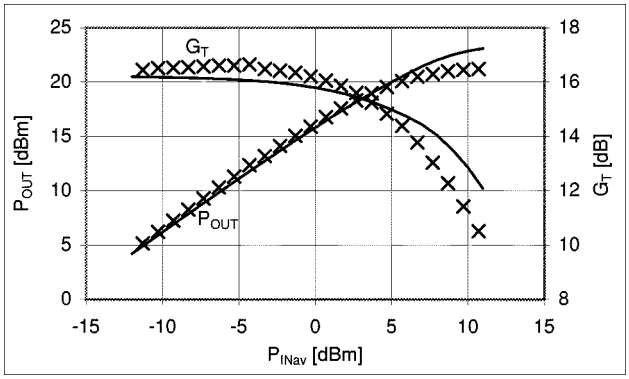

Fig. 6. Output power $P_{\rm out}$ and gain $G_{\rm T}$ of the three-stage power amplifier at 62 GHz ($I_{\rm D} = 250$ mA and $V_{\rm DD} = 3.5$ V). Simulated (–) and measured ($\times\times$).

in series with the $\lambda/4$ line to prevent very low-frequency oscillations. To avoid gain reduction, the resistance is placed near the transistor because this is a high-impedance node. To reduce low-frequency gain, interstage networks with shorted stubs were used.

On the last steps of the design, EM simulations were used for the main discontinuities characterization (mainly T-junctions and cross junctions), as mentioned in Section III.

B. Balanced Amplifier

Finally, to increase the output power, two three-stage amplifiers in a balanced configuration were used. To increase bandwidth, Lange couplers were employed. The balanced amplifier final layout is presented in Fig. 4.

The wire bond for integration into an MBS system was taken into account on the input and output matching. Consequently, the amplifier is not 50-Ω matched. Special care was taken to avoid loop oscillation [15]. Due to the Lange couplers isolation, the loop gain is very low (< -30 dB).

V. Experimental Results

A. Three-Stage Amplifier

On-wafer measurements were performed with a probe station and a vector network analyzer. S-parameters measurements were made using a thru-reflect line (TRL) on-wafer calibration kit. Fig. 5 presents measured and simulated small-signal S-parameters for the three-stage power amplifier. Simulations were performed with both electrical [3] and EM [14] discontinuities models for T-junctions and cross junctions and the transistor C-model presented in Section II.

It is noted that it is very important to have a better model for the discontinuities of the microstrip T-junction and crosses.

Fig. 6 presents simulated and measured transducer gain $G_{\rm T}$ and output power $P_{\rm OUT}$ at 62 GHz versus available input power $P_{\rm INav}$. Large-signal measurements were made on wafer with a Gunn diode oscillator (maximum input power available on wafer was 10.7 dBm). An output saturated power of 21 dBm for a compressed gain of 11 dB and almost 18 dBm at 1-dB compression point were measured. The small-signal gain is greater than 16 dB.

The main specification of the amplifier was 20 dBm of output power with high linearity to obtain the MBS demonstrator needed cell coverage [1]. Although efficiency was not the design major goal, values of 13.1% and 16% were measured with $V_{\rm DS} = 3.5$ V and 2.5 V, respectively.

The very good agreement between the simulations and experiments with large signals validates the modeling technique well beyond the 1-dB compression point.

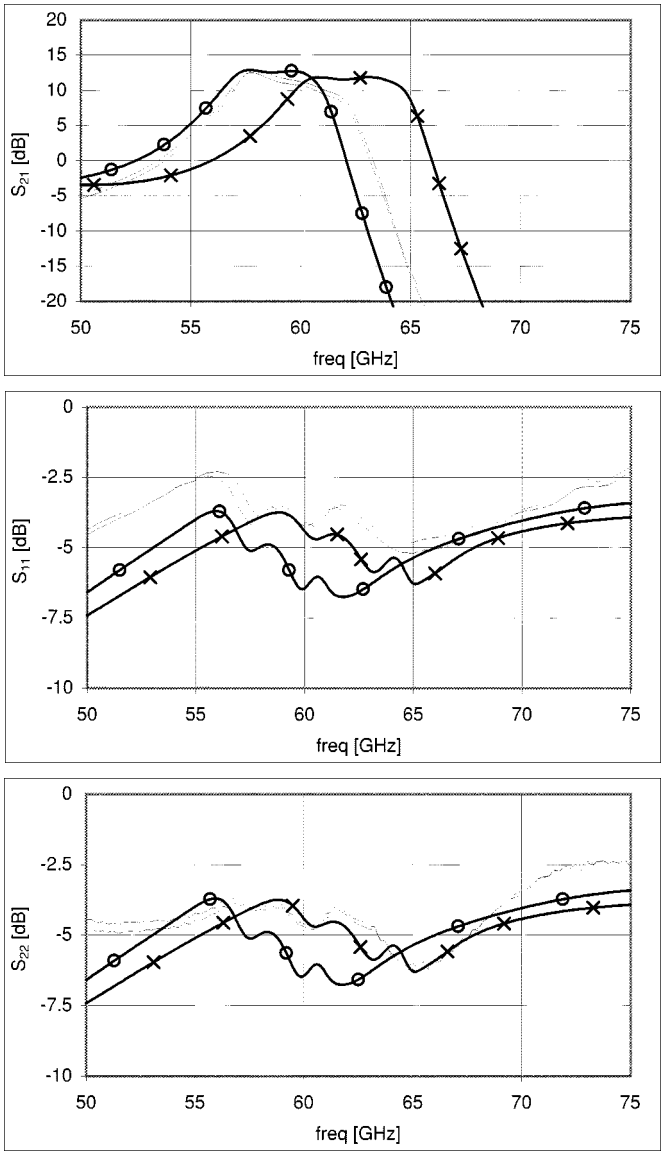

Fig. 7. S-parameters of the balanced amplifier ($I_{\rm D} = 480$ mA and $V_{\rm DD} = 3.5$ V). Experimental results of two chips of the same wafer (—), simulations with EM discontinuities models (–o–), and with MDS discontinuities models (–×–).

B. Balanced Amplifier

Fig. 7 presents measured and simulated small-signal scattering parameters for the balanced amplifier. Simulations were performed with the C-model using electrical [3] and EM discontinuities [14] models.

As with the three-stage amplifier, we also notice a good agreement between measurements and simulations when the EM model is used for the microstrip discontinuities. The balanced amplifier presents low-input and low-output return loss. This comes as a result of it been matched for integration (the wire bonding and their parasitic were included on the amplifier design) and the measurements were performed on wafer with a 50-Ω calibration kit.

Fig. 8 presents simulated and measured transducer gain $G_{\rm T}$ and output power $P_{\rm OUT}$ at 62 GHz versus available input power $P_{\rm INav}$. An output power around 20 dBm for a compressed gain of 9 dB and almost 18 dBm at a 1-dB compression point was measured. The small-signal gain is greater than 12 dB.

The cascade and balanced amplifiers have similar 1-dB compression points and the small-signal gain of the cascade amplifier is 4 dB

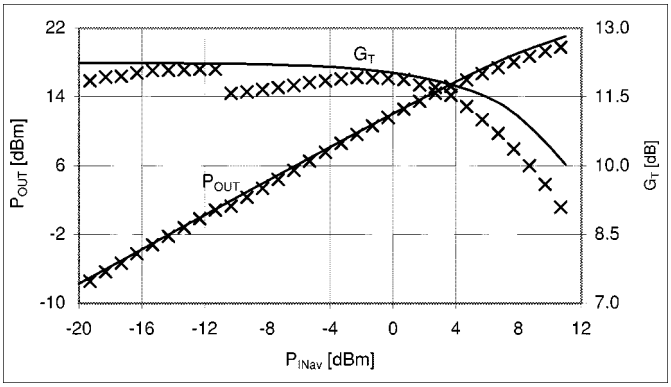

Fig. 8. Simulated (—) and measured ($\times\times$) output power $P_{\rm out}$ and gain $G_{\rm T}$ of the balanced power amplifier at 62 GHz ($I_{\rm D} = 480$ mA and $V_{\rm DD} = 3.5$ V).

higher. This is due to the balanced amplifier 50-Ω mismatch and the Lange couplers insertion losses. On tested Lange couplers, 0.5–1-dB insertion losses were measured at 62 GHz [13]. Accordingly, on the waveguide carrier, an increase of 1.5 dB was measured for $P_{\rm OUT}$. The saturated output power of this amplifier was not reached due to the lack of on-wafer input power.

VI. Conclusions

Two V-band monolithic-microwave integrated-circuit (MMIC) power amplifiers were designed, fabricated, and tested. A new PMHFET large-signal model based on continuous dc and ac measurements was presented (C-model). For comparison purposes, S-parameters measurements and simulations using the proposed model and another one based on pulsed measurements up to 20 GHz (P-model), were performed from 1 to 75 GHz. The poor accuracy of the P-model may be partially associated with different bias conditions used on its model parameters extraction and also to the lower frequency band where pulsed measurements were made since the available pulsed measurements bench has a frequency limit of 20 GHz.

It was shown that at 60 GHz, better models than those available on commercial software for some microstrip discontinuities, mainly T-junctions and cross junctions, were needed. In this paper, those models were obtained with an EM simulator.

The simulated results with the proposed PMHFET large-signal model show a very good agreement with experiments not only on the small signal, but also on the output power. A 21-dBm output power with a 16% power-added efficiency at 62 GHz was obtained with a three-stage amplifier. With a balanced amplifier, a 1-dB compression point of 18 dBm was measured on wafer and 19.5 dBm on test jig. Higher output power levels can be achieved with a saturated class-A operation.

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